

EAST SEARCH

11/14/2007

L#	Hits	Search String	Databases	
L1	26	((logic and gate and delay adj time) and rise and fall) and logical adj operation) ai USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L2	5	((logic and gate and delay adj time) and rise and fall) and logical adj operation) ai USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L3	8	((logic and gate and delay adj time) and rise and fall) and logical adj operation) ai USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L4	46970	hassegawa.in. hassegawa.in. and delay	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L5	956	hassegawa.in. and delay	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L6	121	(hassegawa.in. and delay) and NEC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L7	45	(hassegawa.in. and delay) and NEC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L1	12	((hassegawa.in. and delay) and NEC) and rise and fall	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L2	1628	delay adj calculat\$ look adj3 table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L3	26127	((delay adj calculat\$) and (look adj3 table)) and library	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L4	74	((delay adj calculat\$) and (look adj3 table)) and library	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L5	3	((delay adj calculat\$) and gate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L6	473	((delay adj calculat\$) and gate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L7	67	((delay adj calculat\$) and gate) and fall and rise	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L8	38	((delay adj calculat\$) and gate) and fall and rise) and simulat\$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L9	29	((Blinne and delay time) and logic cell) and rise/fall) and estimating	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
	7	optimizing adj signal adj timing	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
106402		logic adj circuit\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
		((logic adj circuit\$1) and (calculat\$3 adj delay)) and (logic\$2 adj (information or op USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
		37	((logic adj circuit\$1) and (calculat\$3 adj delay)) and (logic\$2 adj (information or op USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		112	((logic adj circuit\$1) and (comput\$5 adj delay)) and (estimat\$3 adj delay)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		96	((logic adj circuit\$1) and (estimat\$3 adj delay))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		468	((logic adj circuit\$1) and (calculat\$3 adj delay)) or ((logic adj circuit\$1) and (comput USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		56	((logic adj circuit\$1) and (calculat\$3 adj delay)) or ((logic adj circuit\$1) and (comput USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		7	((logic adj circuit\$1) and (calculat\$3 adj delay)) and ((logic\$2 adj (information or op USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		5	((logic adj circuit\$1) and (calculat\$3 adj delay)) or ((logic adj circuit\$1) and (comput USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		11	((logic adj circuit\$1) and (calculat\$3 adj delay)) or ((logic adj circuit\$1) and (comput USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
33722		logic adj gate\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
		17.9	((logic adj gate\$1) and (calculat\$3 adj delay))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		47	((logic adj gate\$1) and (comput\$5 adj delay))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		61	((logic adj gate\$1) and (estimat\$3 adj delay))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		268	((logic adj gate\$1) and (calculat\$3 adj delay)) or ((logic adj gate\$1) and (comput\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		38	((logic adj gate\$1) and (calculat\$3 adj delay)) or ((logic adj gate\$1) and (comput\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		0	((logic adj gate\$1) and (delay with library)) and ("connection information" or "connection information" or "circi USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		220	((logic adj circuit\$1) and (delay with library)) and ("connection information" or "connection information" or "circi USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
		46	((logic adj circuit\$1) and (delay with library)) and ("connection information" or "connection information" or "circi USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

0 (((logic adj circuit\$1) and (delay with library)) and ("connection information" or "cir USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
10 ((logic adj circuit\$1) and (delay with library)) and ("connection information" or "cir USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
220 (logic adj circuit\$1) and (delay with library)
11 ((logic adj circuit\$1) and (delay with library)) and "logic information"

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Hasegawa

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<u>Results of search set L32:(logic adj gate\$1) and ((calculat\$3 adj delay) or (comput\$5 adj delay) or (estimat\$3 adj delay)) and (logic\$2 adj (information or operation))</u>			
Document	II Title	Source	Issue Date Current OR
US 2003006816 A1	Semiconductor integrated circuit device and microcomputer	20030109 327/158	
US 20020113616 A1	Semiconductor integrated circuit	20020822 326/31	
US 20020030521 A1	Semiconductor integrated circuit device and microcomputer	20020314 327/158	
US 20020008560 A1	Variable delay circuit and semiconductor integrated circuit device	20020124 327/277	
US 2001043103 A1	Semiconductor integrated circuit	20011122 327/175	
US 2001043085 A1	Semiconductor integrated circuit	20011122 326/112	
US 2001024136 A1	Semiconductor integrated circuit compensating variations of delay time	20010927 327/276	
US 2001015658 A1	Semiconductor integrated circuit device capable of producing output thereof without being influenced by of	20010823 326/104	
US 6477695 B1	Methods for designing standard cell transistor structures	20021105 716/17	
US 64776683 B1	Automated processor generation system for designing a configurable processor and method for the same	20021105 716/1	
US 6476639 B2	Semiconductor integrated circuit device capable of producing output thereof without being influenced by of	20021105 326/82	
US 6472916 B2	Semiconductor integrated circuit device and microcomputer	20021029 327/158	
US 6388483 B1	Semiconductor integrated circuit device and microcomputer	20020514 327/158	
US 6380778 B2	Semiconductor integrated circuit	20020430 327/175	
US 6304117 B1	Variable delay circuit and semiconductor integrated circuit device	20011016 327/158	
US 6301692 B1	Method for designing layout of semiconductor integrated circuit, semiconductor integrated circuit obtained	20011009 716/10	
US 6295300 B1	Circuit and method for symmetric asynchronous interface	20010925 370/503	
US 6215345 B1	Semiconductor device for setting delay time	20010410 327/279	
US 6181184 B1	Variable delay circuit and semiconductor intergrated circuit device	20010130 327/278	
US 6166577 A	Semiconductor integrated circuit device and microcomputer	20011226 327/278	
US 6097884 A	Probe points and markers for critical paths and integrated circuits	20000801 716/4	
US 5983008 A	Method for designing layout of semiconductor integrated circuit, semiconductor integrated circuit obtained	19991109 716/6	
US 5923569 A	Method for designing layout of semiconductor integrated circuit semiconductor integrated circuit obtained t	19990713 716/7	
US 5764525 A	Method for improving the operation of a circuit through iterative substitutions and performance analyses of	19980609 716/18	
US 5661413 A	Processor utilizing a low voltage data circuit and a high voltage controller	19970826 326/80	
US 5619418 A	Logic gate size optimization process for an integrated circuit whereby circuit speed is improved while circui	19970408 716/6	
US 5613062 A	Logic simulator	19970318 714/37	
US 5606567 A	Delay testing of high-performance digital components by a slow-speed tester	19970225 714/732	
US 5600583 A	Circuit and method for detecting if a sum of two multidigit numbers equals a third multidigit number prior to	19970204 708/525	
US 5508950 A	Circuit and method for detecting if a sum of two multibit numbers equals a third multibit constant number pi	19960416 708/525	

US 5446748 A
US 5426591 A
US 5270955 A
US 5124776 A
US 5001751 A
US 4926478 A
US 4805216 A
US 3914580 A

Apparatus for performing logic simulation
Apparatus and method for improving the timing performance of a circuit
Method of detecting arithmetic or logical computation result
Bipolar integrated circuit having a unit block structure
Mode 4 reply decoder
Method and apparatus for continuously acknowledged link encrypting
Method and apparatus for continuously acknowledged link encrypting
TIMING CONTROL CIRCUIT FOR ELECTRONIC FUEL INJECTION SYSTEM

19950829 714/814
19950620 716/6
19931214 708/525
19920623 257/204
19910319 342/45
19900515 705/75
19890214 380/283
19751021 377/2